

AMENDMENTS TO THE CLAIMS

Listing Of Claims

Claims 1-46 (Canceled)

47. (currently amended) A semiconductor component comprising:

a semiconductor die comprising a face and a plurality of die contacts on the face in a pattern; and
a redistribution circuit on the face comprising:

a plurality of conductors ~~on the face~~ in electrical communication with the die contacts configured to redistribute the pattern of the die contacts;

a plurality of first contacts ~~on the face~~ in electrical communication with the conductors configured for flip chip mounting the component to a supporting substrate; and

a plurality of second contacts ~~on the die contacts~~ in electrical communication with the conductors configured for electrical contact by a test probe.

48. (previously presented) The component of claim 47 wherein the first contacts comprise bumps in an area array.

49. (previously presented) The component of claim 47 further comprising an under bump metallization layer on each first contact.

50. (currently amended) The component of claim 47 wherein the second contacts comprise pads comprising a non-oxidizing metal.

51. (currently amended) The ~~semiconductor~~ component of claim 47 wherein the component is contained on a wafer.

52. (previously presented) The component of claim 47 further comprising an electrically insulating layer between the die and the conductors.

53. (previously presented) The component of claim 47 wherein the conductors are configured to fan out or to fan in the pattern of the die contacts.

54. (currently amended) A semiconductor component comprising:

a semiconductor die having a face and a plurality of die contacts on the face in a pattern; and

a redistribution circuit on the face comprising:

a plurality of conductors ~~on the face~~ in electrical communication with the die contacts configured to redistribute the pattern of the die contacts;

an electrically insulating layer on the conductors having a plurality of openings aligned with the die contacts;

a plurality of first contacts ~~on the face~~ in electrical communication with the conductors configured for flip chip mounting the component to a supporting substrate; and

a plurality of second contacts ~~on the face~~ in electrical communication with the conductors comprising pads in the openings configured for electrical contact with a test probe.

55. (previously presented) The component of claim 54 wherein the pads comprise portions of the conductors.

56. (previously presented) The component of claim 54 wherein the component comprises a semiconductor wafer.

57. (previously presented) The ~~semiconductor~~ component of claim 54 wherein the first contacts comprise balls in a ball grid array and each ball of the ball grid array is in electrical communication with a second contact.

58. (currently amended) A semiconductor component comprising:

a semiconductor wafer;

a plurality of components on the wafer, each component comprising ~~a face and~~ a plurality of die contacts ; ~~on the face,~~

each component further comprising a redistribution circuit ~~on the face~~ comprising:

a plurality of conductors in electrical communication with the die contacts configured for signal transmission in the component and to redistribute a pattern of the die contacts;

a plurality of test contacts ~~on the face~~ comprising non-oxidizing layers on portions of the conductors; and

a plurality of terminal contacts ~~on the face~~ in electrical communication with the conductors.

59. (currently amended) The component of claim 58 wherein the terminal contacts comprise under bump

metallization layers and solder bumps configured for flip chip mounting the component to a supporting substrate.

60. (previously presented) The component of claim 58 further comprising an electrically insulating layer on the redistribution circuit having a plurality of openings aligned with the test contacts.

61. (previously presented) The component of claim 58 wherein the test contacts comprise portions of the conductors.

62. (currently amended) The component of claim 58 wherein the test contacts are configured for electrical engagement by a test probe ~~comprises~~ comprising a needle probe, a buckle beam probe, a spring segment probe or a silicon probe.

63. (currently amended) A semiconductor component comprising:

a semiconductor die comprising a face and a plurality of die contacts on the face; and
~~in a pattern;~~

a redistribution circuit on the face comprising:

a plurality of redistribution conductors ~~on the face~~ in electrical communication with the die contacts;

a plurality of bumped terminal contacts; and

~~on the face comprising under bump metallization layers on the conductors; and~~

a plurality of test contacts ~~on the face~~ comprising non oxidizing layers on the conductors aligned with the die contacts.

64. (previously presented) The component of claim 63 wherein the die is contained on a semiconductor wafer containing a plurality of dice substantially similar to the die.

65. (currently amended) The component of claim 63 wherein the bumped terminal contacts comprise solder balls in a grid array configured for flip chip mounting the component to a supporting substrate.

66. (previously presented) The component of claim 63 wherein the test contacts comprise portions of the redistribution conductors.

67. (previously presented) The component of claim 63 wherein the non oxidizing layers comprise a metal selected from the group consisting of Au and Pt.